




## Faculty Profile on University Website

www.mjpru.ac.in

Title	Dr.	First Name	Yograj Singh	Last Name	Daksh	Photograph
Designation		Professor				
Department		Electronics & Instrumentation Engineering				
Address	Campus	Faculty of Engineering & Technology M.J.P. Rohilkhand University, Bareilly-243006, India				
	Residence	13/A, Amber, Supercity, Bareilly-243006				
Mobile No.		7906553046				
Email ID		Personal		yograj.siet@gmail.com		
		University Domain		ysdaksh.ei@mjpru.ac.in		
Professional Networking ID, i.e. LinkedIn, Twitter etc.		LinkedIn: <a href="https://www.linkedin.com/in/dr-yograj-singh-97b49116/">https://www.linkedin.com/in/dr-yograj-singh-97b49116/</a>				
Educational Qualifications (Post Graduation Onwards)						
Course/Degree		Institution		Year	Details/Thesis Topic/Subjects	
M.Sc. (Physics)		Rohilkhand University, Bareilly		1996	Specialization-Electronics	
M. Phil (Instrumentation)		University of Roorkee (now IIT Roorkee), Roorkee		1999	A Structural Tilt Measurement System	
M. Tech. (Instrumentation Engineering)		Regional Engineering College (now NIT, Kurukshetra) Kurukshetra		2001	A Study of Interconnect Parasitics in VLSI-chips	
Ph. D. (Electronics Engineering)		Shobhit University, Meerut (Deemed University U/S 3 of UGC Act 1956)		2016	Crosstalk and Propagation Delay Analysis in Modern VLSI Interconnects	
Career Profile						
Organization / Institution			Designation	Duration	Nature of Duties	
M.J.P. Rohilkhand University, Bareilly			Professor	17 April 2016 onwards	Academic, Administrative & Research	
M.J.P. Rohilkhand University, Bareilly			Associate Professor	29 Sept., 2011 to 16 April, 2016	Academic, Administrative & Research	
M.J.P. Rohilkhand University, Bareilly			Reader	29 Sept., 2008 to 28 Sept., 2011	Academic & Research	
Shobhit University, Meerut (Deemed University U/S 3 of UGC Act 1956)			Assistant Professor	01 Aug, 2007 to 28 Sept, 2008	Academic & Research	
Shobhit Institute of Engineering & Technology, Meerut			Lecturer /Sr. Lecturer	5 Aug, 2005 to 31 July, 2007	Academic	
Teerthanker Mahaveer Institute of Management & Technology, Moradabad			Lecturer	21 Feb, 2002 to 04 Aug, 2005	Academic	

<b>Research Interests / Specialization</b>									
<ul style="list-style-type: none"> <li>Modeling of Hybrid VLSI Interconnects</li> <li>Modeling and Simulation of CNT/GNR based VLSI Interconnects</li> <li>Modeling and Simulation of Junctionless FETs</li> <li>Instrumentation Systems and Measurement Techniques</li> </ul>									
<b>Research Experience in Years:</b> 15 years									
<b>No of Research Scholars :</b> 01 (Ongoing)									
Name of Programme		Awarded			Under Supervision				
Ph.D.		Ongoing			me				
<b>Researcher/ Expert ID</b>	<b>Scopus</b>	<b>Orchid</b>		<b>Publons</b>	<b>Vidwan</b>	<b>Google Scholar</b>			
	36805538500	0000-0002V-5004-7283		AAZ-5057-2020	165546	EQU0KHIAAAAJ			
<b>Total Teaching Experience (Subjects/Courses Taught):</b> 21 Years									
Solid State Electronic Devices; Industrial Instrumentation; Linear Integrated Circuits; Integrated Circuit Technology & Design; Biomedical Instrumentation; Electronic Measurement & Instrumentation; Electronics Engineering Materials; Transducers, Sensors & Display Devices; VLSI Technology; VLSI Deign; Digital Electronics etc.									
<b>Honours / Awards &amp; Fellowship for outstanding work:</b> No, Please.									
<b>Name of Award/ Fellowship</b>		<b>Awarded By</b>							
		<b>Name of Governmental Agency</b>	<b>Name of Government Supported Organization/ Department</b>			<b>Name of International Recognized Body</b>			
<b>Publications /Academic Activities (Numbers Only)</b>									
Books & Monographs (Single Author)	No	Research Papers Published in International Journals	06	Papers Presented in Seminars/ Conferences	01	Seminars/ Conferences Organized	No	Research Projects (Completed)	02
Books (Co-authored)	No	Research Papers Published in Other Journals	No	Seminar/ Conferences Attended	02	Workshops Organized	No	Research Projects (Ongoing)	01
Books (Edited)	No	Articles Published in Popular Fora, e.g., Websites, Blogs, Newspapers, Magazines etc.	No	Sessions Chaired in Seminars/ Conferences	No	Membership of Academic/ Professional Bodies	06	Foreign Countries Visited for Academic Assignments	No
Chapters in Edited Books	No			Resource Lectures Delivered	No				

Details of Publications /Academic Activities (2010 Onwards)								
(a) Authored Books/ Monographs: No, Please.								
Name of Book		Year of Publication		Publisher		ISBN No		
(b) Edited Books: No, Please.								
Year of Publication	Title		Publisher	ISBN	DOI No.	Citations		
(c) Papers Published in UGC Care Listed /Indexed/ Peer Reviewed Journals								
Year of Publication	Title		Name of Journal		ISSN No.	Citations	Impact Factor	
2010	Performance comparison of carbon nanotubes, nickel silicide nanowire and copper VLSI interconnects: perspectives and challenges ahead.		Journal of Engineering, Design and Technology, Emerald, Vol. 8, No. 3, pp. 334-353, 2010.		1726-0531	07	0.76	
2013	Analysis of Propagation Delay and Power with Variation in Driver Size and Number of Shells in Multi Walled Carbon Nanotube Interconnects.		Journal of Engineering, Design and Technology, Emerald, Vol. 11, No. 1, pp. 19-33, 2013.		1726-0531	09	0.76	
2015	FDTD technique based crosstalk analysis of bundled SWCNT interconnects.		Journal of Semiconductors, IOP, Vol. 36, No. 5, pp. 055002-1-55002-9, 2015.		1674-4926	21	1.18	
2018	Delay and Power Analysis of Bundled SWCNT Interconnects with variation in driver size.		International Journal of Research in Electronics and Computer Engineering, Vol.6, No.4, pp. 860-866, 2018		2393-9028			
2020	Subthreshold Modeling of Graded Channel Double Gate Junctionless FETs		Silicon Journal, Springer, Vol. 13, Issue: 04 (April 2021), pp. 1231-1238, 2020 Published online: 25 May, 2020		1876-9918	07	3.4	
2021	Self-heating and Negative Differential Conductance Improvement by Substrate Bias Voltage in Tri-gate Junctionless Transistor		Silicon Journal, Springer Published on 04 March, 2021		1876-9918	02	3.4	
(d) Chapter/Paper Published in Edited Books: No, Please								
Publication		Title of the Book	Title of the Chapter	Name & Address of Publisher	Year	ISBN	DOI	Citation Google/ web of science
National	International							
3								
(e) Invited as Resource Lectures Person/Examiner/Expert								

Resource person	Detail of Event	Title of Lecture	Date	Institution	
External Examiner	To conduct the dissertation viva-voce of M. Tech. Students	-	2018 to 2019	GBPUAT, Pantnagar, (Uttarakhand)	
External Examiner	To conduct external Lab Examinations	-	2010 to 2018	FET, Gurukul Kangri University, Haridwar (Uttarakhand)	
Paper setter	at B.Tech Level	-	2016, 2018	FET, Gurukul Kangri University, Haridwar (Uttarakhand)	
Paper Setter	at B.Tech Level	-	2015 to 2018	College of Technology, Teerthanker Mahaveer University, Moradabad	
(f) Seminars/Conferences/Workshops Attended/Organized:					
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Co-Coord inator	Atal Centre for Artificial Intelligence	2022 Onwards	-
Nodal Office r	Anti Narcotics Task Force	2023 onwards	-
<b>(i) Seminar/Conference Presentations</b>			
(1) <b>Yograj Singh Duksh</b> , Brajesh Kumar Kaushik, Sankar Sarkar and Rajendra Prasad Agarwal, "Effect of Driver Size and Number of Shells on Propagation Delay in MWCNT Interconnects", in <i>IEEE International Conference on Devices &amp; Communications (ICDeCom-2011)</i> , Ranchi, Jharkhand, February 24 -25, 2011.			
<b>(j) Memberships of Academic/Professional Bodies</b>			
(1) Senior Member of 'Institute of Electrical and Electronics Engineers' (IEEE) : SM-97206502			
(2) Fellow of 'The Institution of Electronics and Telecommunication Engineers' (IETE) : F-501674			
(3) Fellow of 'The Institution of Engineers India' (IEI) : F-1271020			
(4) Life Member of 'The Indian Society of Technical Education' (ISTE) : LM-69993			
(5) Life Member of 'Instrument Society of India' (ISOI) : LM-1935			
(6) Annual Member of 'Indian Physics Association' (IPA) : AM/35			
<b>(k) Participation in Community Service / Exchange Programme / Consulting Activity:</b> No, Please			
<b>(l) International Academic Exposure:</b> No, Please.			
<b>(m) Any Other Details:</b>			
(1) Qualified Graduate Aptitude Test in Engineering (GATE-1999) and got scholarship by MHRD from 1999 to 2001 during M.Tech. Program.			
(2) Reviewers of the following Journals: (i) Microelectronics Journal (ii) Micro and Nano Letters (iii) Arabian Journal for Science and Engineering			
<b>References:</b> (I) Prof. Brajesh Kumar Kaushik Department of Electronics & Communication Engineering Indian Institute of Technology, Roorkee  (II) Prof. Rajendra P. Agarwal (Ex. Vice Chancellor, Bundelkhand University, Jhansi) Academic Advisor, Shobhit University, Meerut Retd. Prof & Head, Department of Electronics & Communication Engineering Indian Institute of Technology, Roorkee			

(Dr.Yograj Singh Daksh)  
Name & Signature of Faculty Member